11.3 Gbps, Active Back-Termination, Differential Laser Diode Driver

Data Sheet **ADN2531**

FEATURES

3.3 V operation
Up to 11.3 Gbps operation
Typical 26 ps rise/fall times
Bias current range: 10 mA to 100 mA
Differential modulation current range: 10 mA to 80 mA
Voltage input control for bias and modulation currents
Data inputs sensitivity: 150 mV p-p differential
Automatic laser shutdown (ALS)
Crosspoint adjustment (CPA)
VCSEL, FP, DFB laser support
SFF/SFP/XFP/SFP+ MSA compliant
Optical evaluation board available
Compact, 3 mm × 3 mm LFCSP

APPLICATIONS

Optical transmitters, up to 11.3 Gbps, for SONET/SDH, Ethernet, and Fibre Channel applications
SFF/SFP/SFP+/XFP/X2/XENPAK/XPAK MSA compliant
300-pin optical modules, up to 11.3 Gbps

GENERAL DESCRIPTION

The ADN2531 laser diode driver can work with directly modulated laser diodes, including vertical-cavity surface-emitting laser (VCSEL), Fabry-Perot (FP) lasers, and distributed feedback (DFB) lasers, with a differential loading resistance ranging from 5 Ω to 140 Ω. The active back-termination in the ADN2531 absorbs signal reflections from the laser diode side of the output transmission lines, enabling excellent optical eye quality even when the TOSA end of the output transmission lines is significantly mismatched. The ADN2531 is a SFP+ MSA-compliant device, and small package and enhanced ESD protection provides the optimum solution for compact modules in which laser diodes are packaged in low pin-count optical subassemblies.

The modulation and bias currents are programmable via the MSET and BSET control pins. By driving these pins with control voltages, the user has the flexibility to implement various average optical power and extinction ratio control schemes, including a closed-loop or a look-up table control. The automatic laser shutdown (ALS) feature allows turning the bias on and off while simultaneously modulating currents by driving the ALS pin with a low voltage transistor-to-transistor logic (LVTTL) source.

The product is available in a space-saving, 3 mm × 3 mm LFCSP package and operates from −40°C to +100°C.

FUNCTIONAL BLOCK DIAGRAM

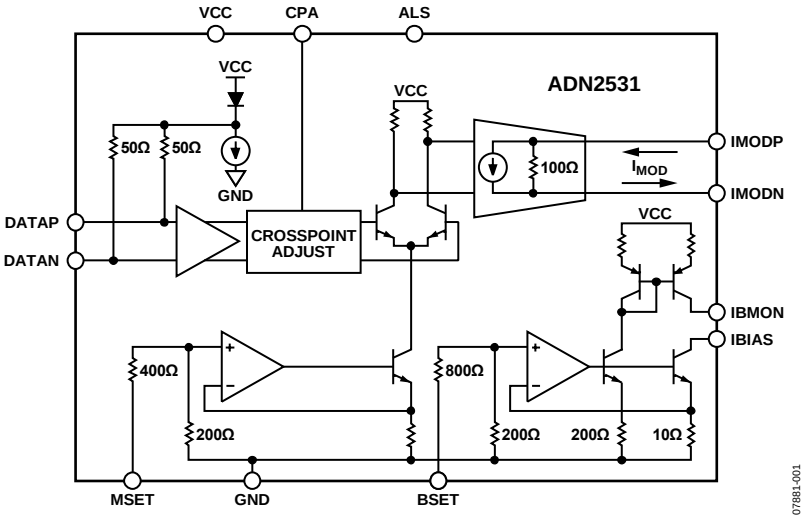

Figure 1.

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COMPARABLE PARTS

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EVALUATION KITS

- ADN2531 Evaluation Board

DOCUMENTATION

Data Sheet

- ADN2531: 11.3 Gbps, Active Back-Termination, Differential Laser Diode Driver Data Sheet

DESIGN RESOURCES

- ADN2531 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

4/2017—Rev. B to Rev. C

Changed CP-16-27 to CP-16-22 ... Throughout
Updated Outline Dimensions ... 18
Changes to Ordering Guide ... 18

9/2016—Rev. A to Rev. B

Changes to Figure 3 ... 6
Updated Outline Dimensions ... 18
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10/2013—Rev. 0 to Rev. A

Updated Outline Dimensions ... 18
Changes to Ordering Guide ... 18

9/2009—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = VCC_{MIN} to VCC_{MAX}, T_A = −40°C to +100°C, 12 Ω differential load impedance, crosspoint adjust disabled, unless otherwise noted. Typical values are specified at 25°C and I_{BIAS} = I_{MOD} = 40 mA with crosspoint adjust disabled, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
BIAS CURRENT (I_{BIAS})					
Bias Current Range	10		100	mA	
Bias Current While ALS Asserted			300	µA	ALS = high
Compliance Voltage[1]	0.6		V_{CC}	V	I_{BIAS} = 80 mA
	0.55		V_{CC}	V	I_{BIAS} = 10 mA
MODULATION CURRENT (IMODP, IMODN)					
Modulation Current I_{MOD} Range	10		80	mA diff	R_{LOAD} = 5 Ω to 50 Ω differential
		70		mA diff	R_{LOAD} = 100 Ω differential
I_{MOD} While ALS Asserted			500	µA diff	ALS = high
Crosspoint Adjust (CPA) Range[2]	35		65	%	
Rise Time (20% to 80%)[2, 3, 4]		26	32.5	ps	
Fall Time (20% to 80%)[2, 3, 4]		26	32.5	ps	
Random Jitter[2, 3, 4]		<0.5		ps rms	
Deterministic Jitter[2, 4, 5]		5.4	8.2	ps p-p	10.7 Gbps, CPA disabled
		5.8	8.2	ps p-p	10.7 Gbps, CPA 35% to 65%
Deterministic Jitter[2, 4, 6]		5.4	8.2	ps p-p	11.3 Gbps, CPA disabled
		5.8	8.2	ps p-p	11.3 Gbps, CPA 35% to 65%
Differential |S22|		−5		dB	5 GHz < f < 10 GHz, Z_0 = 100 Ω differential[7]
		−10.5		dB	f < 5 GHz, Z_0 = 100 Ω differential[7]
Compliance Voltage[1]	V_{CC} − 1.1		V_{CC} + 1.1	V	
DATA INPUTS (DATAP, DATAN)					
Input Data Rate			11.3	Gbps	NRZ
Differential Input Swing	0.15		1.6	V p-p diff	Differential ac-coupled
Differential |S11|		−15		dB	f < 10 GHz, Z_0 = 100 Ω differential
Input Termination Resistance	85	100	115	Ω	Differential
BIAS CONTROL INPUT (BSET)					
BSET Voltage to I_{BIAS} Gain		100		mA/V	
BSET Input Resistance	800	1000	1200	Ω	
MODULATION CONTROL INPUT (MSET)					
MSET Voltage to I_{MOD} Gain		120		mA/V	
MSET Input Resistance		600		Ω	
BIAS MONITOR (IBMON)					
I_{BMON} to I_{BIAS} Ratio		10		µA/mA	
Accuracy of I_{BIAS} to I_{BMON} Ratio	−5.0		+5.0	%	10 mA ≤ I_{BIAS} < 20 mA, R_{IBMON} = 750 Ω
	−4.0		+4.0	%	20 mA ≤ I_{BIAS} < 40 mA, R_{IBMON} = 750 Ω
	−2.5		+2.5	%	40 mA ≤ I_{BIAS} < 70 mA, R_{IBMON} = 750 Ω
	−2		+2	%	70 mA ≤ I_{BIAS} < 80 mA, R_{IBMON} = 750 Ω
AUTOMATIC LASER SHUTDOWN (ALS)					
V_{IH}	2.0			V	
V_{IL}			0.8	V	
I_{IL}	−20		+20	µA	
I_{IH}	0		200	µA	
ALS Assert Time			2	µs	Rising edge of ALS to falling edge of I_{BIAS} and I_{MOD} below 10% of nominal; see Figure 2
ALS Negate Time			10	µs	Falling edge of ALS to rising edge of I_{BIAS} and I_{MOD} above 90% of nominal; see Figure 2

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
V_{CC}	3.0	3.3	3.6	V	
I_{CC}[8]		36		mA	$V_{BSET} = V_{MSET} = 0$ V
I_{SUPPLY}[9]		55	62	mA	$V_{BSET} = V_{MSET} = 0$ V

[1] The voltage between the pin with the specified compliance voltage and GND.
[2] Specified for $T_A = -40°C$ to $+85°C$ due to test equipment limitation. See the Typical Performance Characteristics section for data on performance for $T_A = -40°C$ to $+100°C$.
[3] The pattern used is composed of a repetitive sequence of eight 1s followed by eight 0s at 10.7 Gbps.
[4] Measured using the high speed characterization circuit shown in Figure 22.
[5] The pattern used is K28.5 (00111110101100000101) at 10.7 Gbps rate.
[6] The pattern used is K28.5 (00111110101100000101) at 11.3 Gbps rate.
[7] Measured at balanced IMODP and IMODN.
[8] Only includes current in the ADN2531 VCC pins.
[9] Includes current in ADN2531 VCC pins and dc current in IMODP and IMODN pull-up inductors. See the Power Consumption section for total supply current calculation.

PACKAGE THERMAL SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\theta_{J\text{-}TOP}$	65	72.2	79.4	°C/W	Thermal resistance from junction to top of package.
$\theta_{J\text{-}PAD}$	2.6	5.8	10.7	°C/W	Thermal resistance from junction to bottom of exposed pad.
IC Junction Temperature			125	°C	

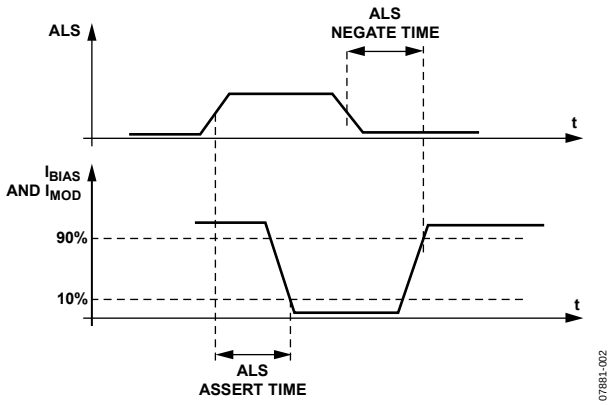

Figure 2. ALS Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage: VCC to GND	−0.3 V to +4.2 V
IMODP, IMODN to GND	VCC − 1.5 V to 4.5 V
DATAP, DATAN to GND	VCC − 1.8 V to VCC − 0.4 V
All Other Pins	−0.3 V to VCC + 0.3 V
ESD on IMODP/IMODN[1]	200 V HBM
ESD on All Other Pins[1]	1.5 kV HBM
Junction Temperature	150°C
Storage Temperature Range	−65°C to +125°C

[1] HBM means human body model.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

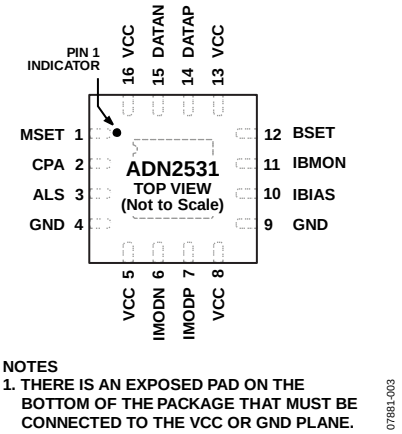

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
1	MSET	Input	Modulation Current Control Input
2	CPA	Input	Crosspoint Adjust Control Input
3	ALS	Input	Automatic Laser Shutdown
4	GND	Power	Negative Power Supply
5	VCC	Power	Positive Power Supply
6	IMODN	Output	Modulation Current Negative Output
7	IMODP	Output	Modulation Current Positive Output
8	VCC	Power	Positive Power Supply
9	GND	Power	Negative Power Supply
10	IBIAS	Output	Bias Current Output
11	IBMON	Output	Bias Current Monitoring Output
12	BSET	Input	Bias Current Control Input
13	VCC	Power	Positive Power Supply
14	DATAP	Input	Data Signal Positive Input
15	DATAN	Input	Data Signal Negative Input
16	VCC	Power	Positive Power Supply
Exposed Pad	EP	Power	Connect to the VCC or GND plane

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.3 V, crosspoint adjust disabled, unless otherwise noted.

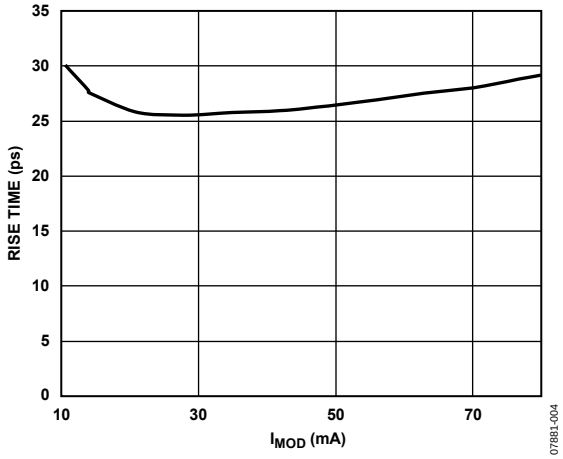

Figure 4. Rise Time vs. I_{MOD}

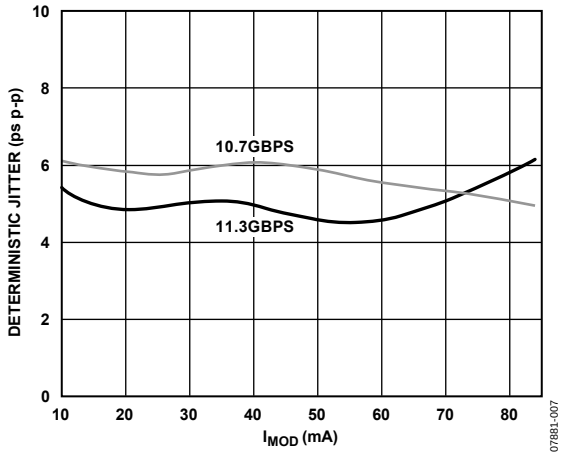

Figure 7. Deterministic Jitter vs. I_{MOD}

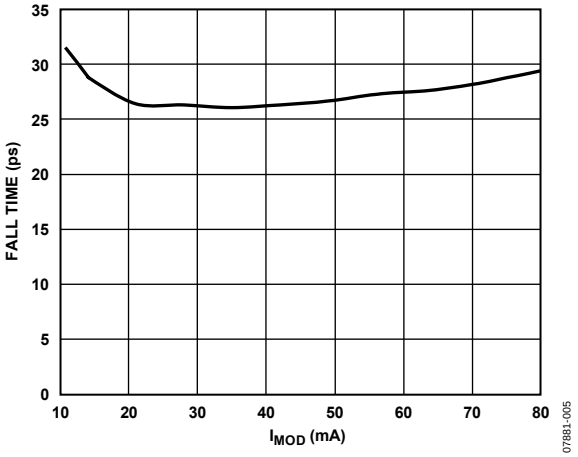

Figure 5. Fall Time vs. I_{MOD}

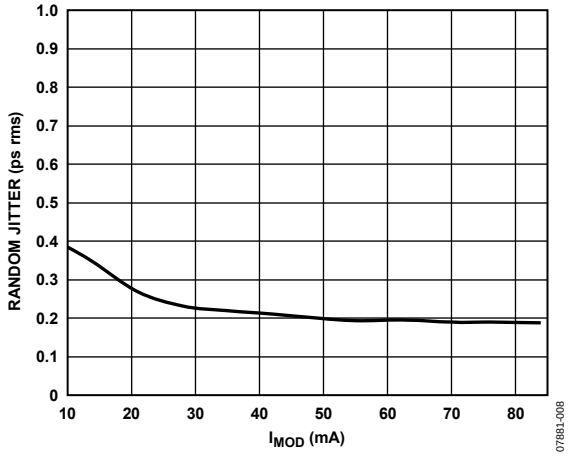

Figure 8. Random Jitter vs. I_{MOD}

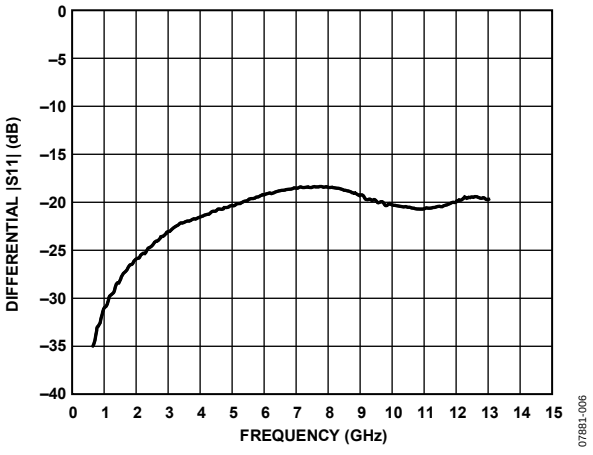

Figure 6. Differential |S11|

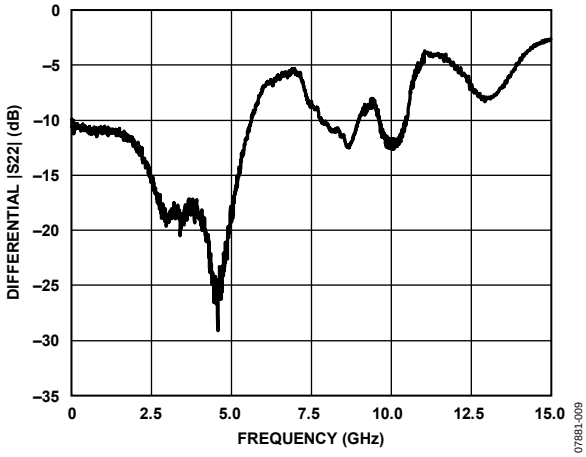

Figure 9. Differential |S22|

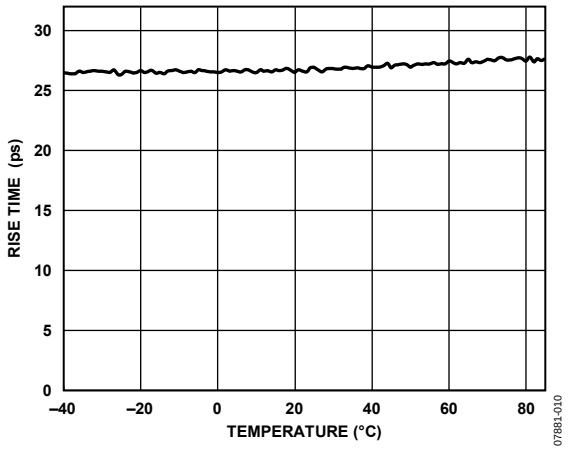

Figure 10. Rise Time vs. Temperature
(Worse-Case Conditions, CPA Disabled)

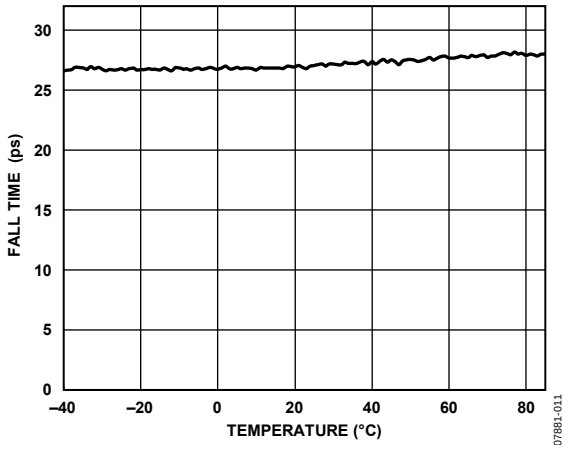

Figure 11. Fall Time vs. Temperature
(Worst-Case Conditions, CPA Disabled)

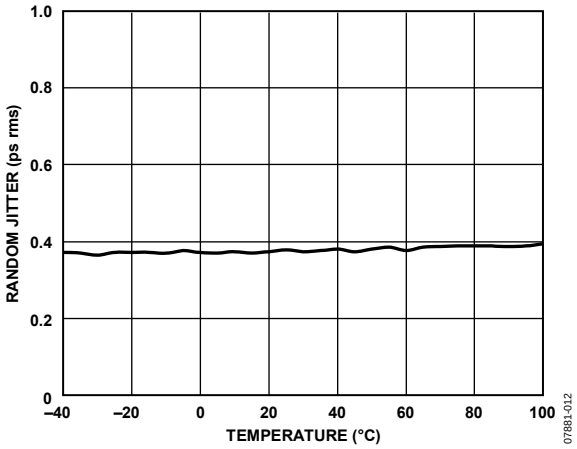

Figure 12. Random Jitter vs. Temperature
(Worst-Case Conditions, CPA Disabled [Worst-Case I_{MOD} = 40 mA])

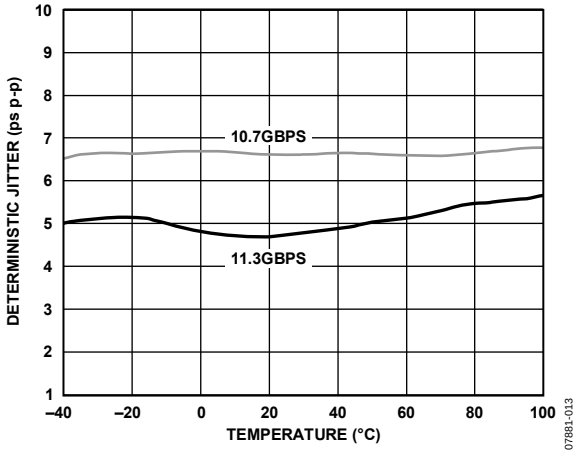

Figure 13. Deterministic Jitter vs. Temperature
(Worse-Case Conditions, CPA Disabled)

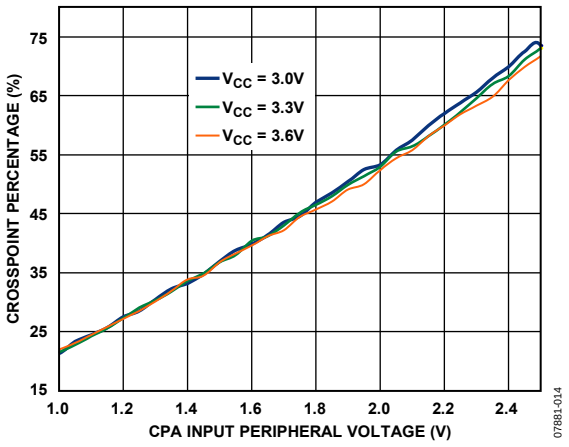

Figure 14. I_{MOD} Eye Diagram Crosspoint vs. CPA Input Peripheral Voltage and V_{CC}
(I_{MOD} = 40 mA)

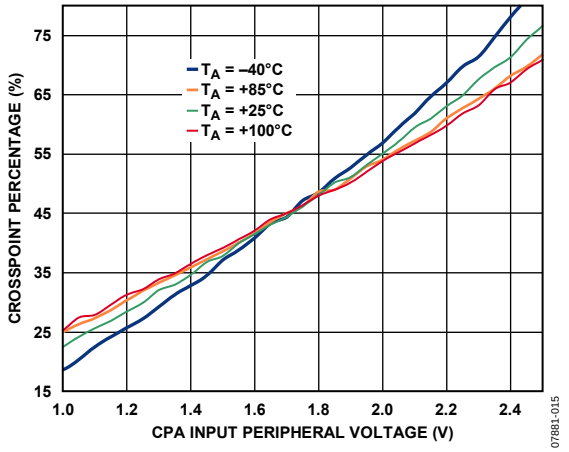

Figure 15. I_{MOD} Eye Diagram Crosspoint vs. CPA Input Peripheral Voltage and
Ambient Temperature (I_{MOD} = 40 mA)

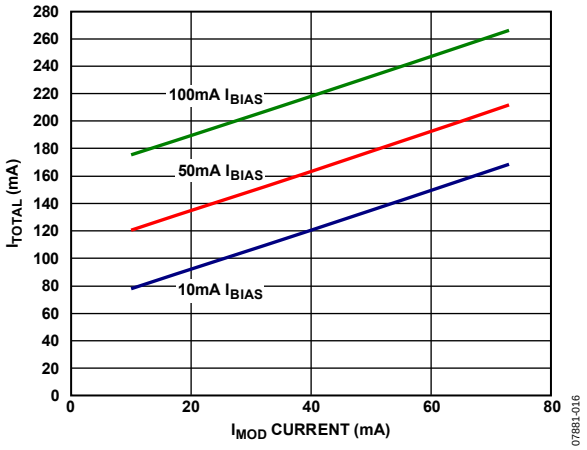

Figure 16. Total Supply Current vs. I_{MOD} and I_{BIAS}

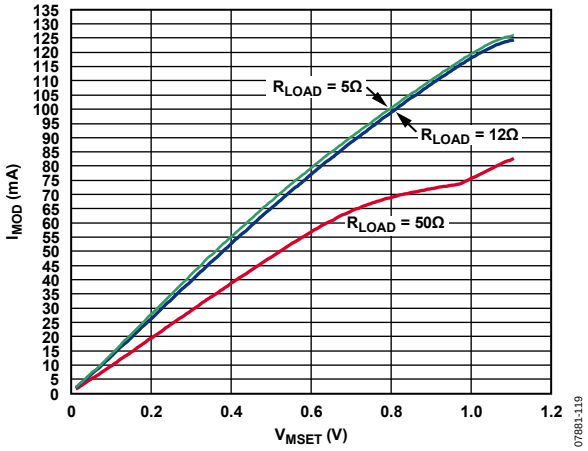

Figure 19. I_{MOD} vs.V_{MSET} at Various R_{LOAD} Resistors

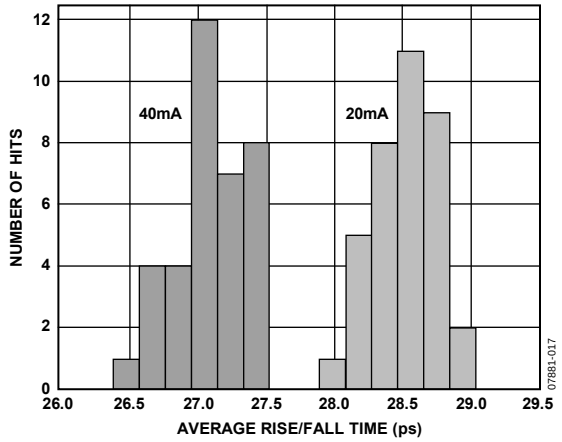

Figure 17. Average Rise/Fall Time Distribution vs. I_{MOD}

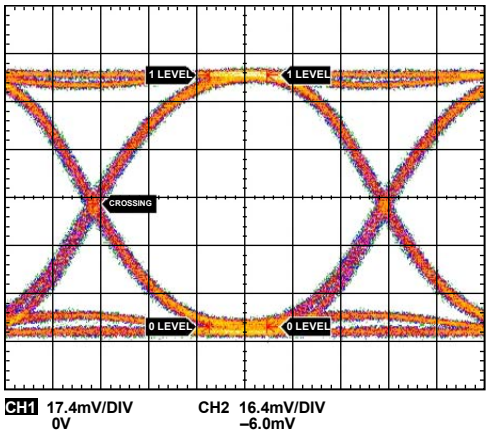

Figure 20. Electrical Eye Diagram
(I_{MOD} = 40 mA, PRBS31 Pattern at 10.3125 Gbps)

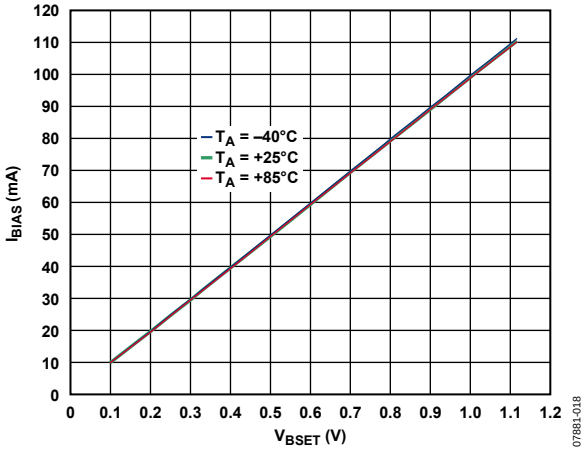

Figure 18. I_{BIAS} vs. V_{BEST} at Various Temperatures

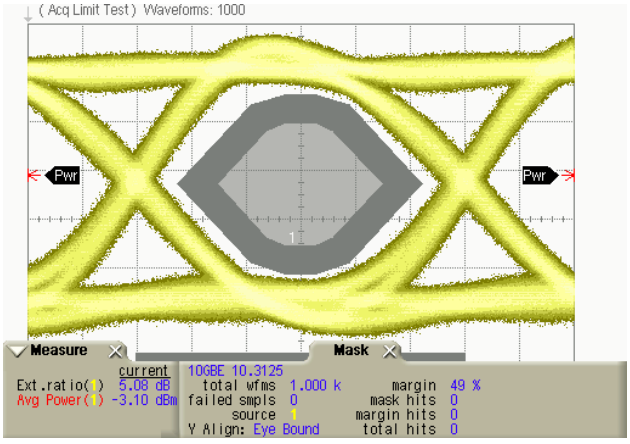

Figure 21. Filtered 10 Gb Ethernet Optical Eye Using NX8346TS DFB (PRBS31 Pattern at 10.3125 Gbps)

TEST CIRCUIT

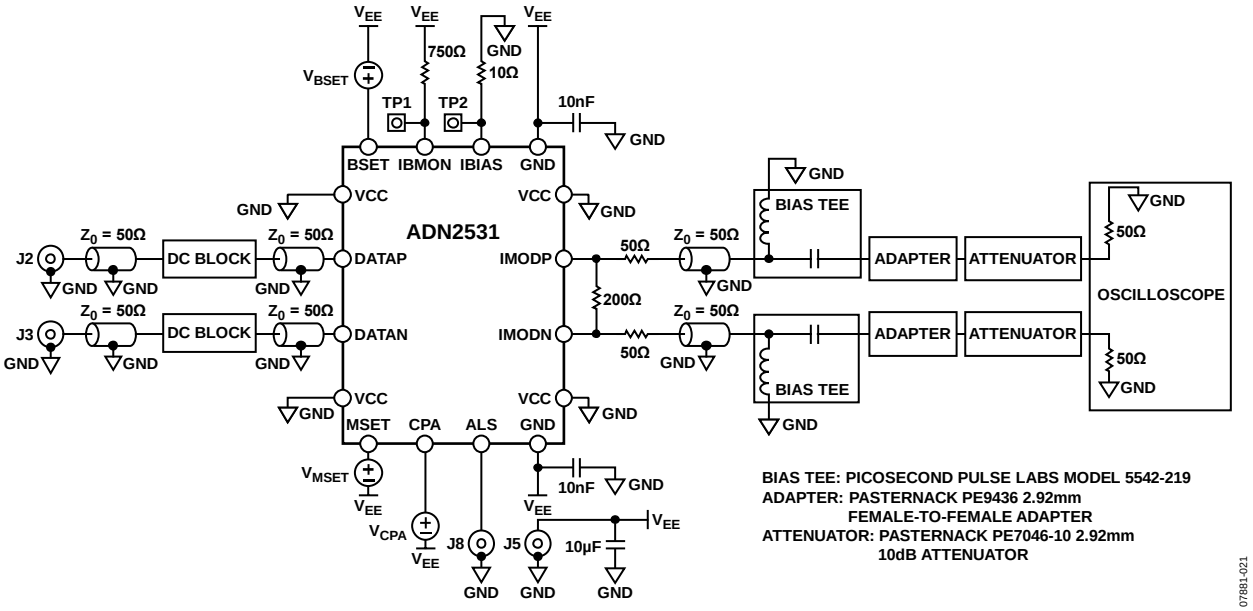

Figure 22. High Speed Characterization Circuit

THEORY OF OPERATION

As shown in Figure 1, the ADN2531 consists of an input stage and two voltage-controlled current sources for bias and modulation. The bias current is available at the IBIAS pin. It is controlled by the voltage at the BSET pin and can be monitored at the IBMON pin. The differential modulation current is available at the IMODP and IMODN pins. It is controlled by the voltage at the MSET pin.

The output stage implements the active back-termination circuitry for proper transmission line matching and power consumption reduction. The ADN2531 can drive a load with differential resistance ranging from 5 Ω to 140 Ω. The excellent back-termination in the ADN2531 absorbs signal reflections from the TOSA end of the output transmission lines, enabling excellent optical eye quality to be achieved even when the TOSA end of the output transmission lines is significantly misterminated.

INPUT STAGE

The input stage of the ADN2531 converts the data signal applied to the DATAP and DATAN pins to a level that ensures proper operation of the high speed switch. The equivalent circuit of the input stage is shown in Figure 23.

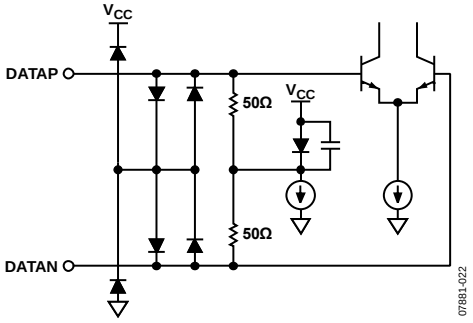

Figure 23. Equivalent Circuit of the Input Stage

The DATAP and DATAN pins are terminated internally with a 100 Ω differential termination resistor. This minimizes signal reflections at the input that can otherwise lead to degradation in the output eye diagram. It is not recommended to drive the ADN2531 with single-ended data signal sources.

The ADN2531 input stage must be ac-coupled to the signal source to eliminate the need for matching between the common-mode voltages of the data signal source and the input stage of the driver (see Figure 24). The ac coupling capacitors must have an impedance less than 50 Ω over the required frequency range. Generally, this is achieved using 10 nF to 100 nF capacitors, for more than 1 Gbps operation.

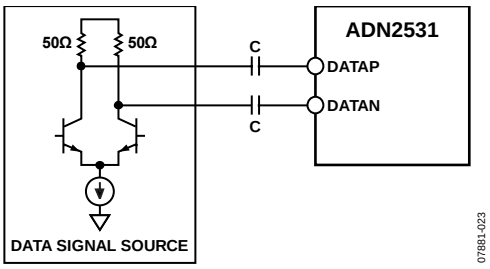

Figure 24. AC Coupling the Data Source to the ADN2531 Data Inputs

BIAS CURRENT

The bias current is generated internally using a voltage-to-current converter consisting of an internal operational amplifier and a transistor, as shown in Figure 25.

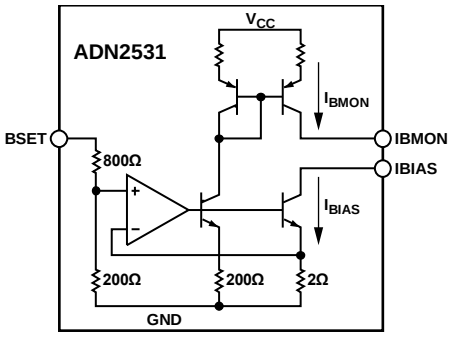

Figure 25. Voltage-to-Current Converter Used to Generate I_{BIAS}

The BSET to I_{BIAS} voltage-to-current conversion factor is set at 100 mA/V by the internal resistors, and the bias current is monitored at the IBMON pin using a current mirror with a gain equal to 1/100. By connecting a 750 Ω resistor between IBMON and GND, the bias current can be monitored as a voltage across the resistor. A low temperature coefficient precision resistor must be used for the IBMON resistor (R_{IBMON}). Any error in the value of R_{IBMON} due to tolerances or drift in value over temperature contributes to the overall error budget for the I_{BIAS} monitor voltage.

If the IBMON voltage is being connected to an ADC for analog-to-digital conversion, R_{IBMON} must be placed close to the ADC to minimize errors due to voltage drops on the ground plane. See the Design Example section for example calculations of the accuracy of the I_{BIAS} monitor as a percentage of the nominal I_{BIAS} value.

The equivalent circuits of the BSET, IBIAS, and IBMON pins are shown in Figure 26 to Figure 28.

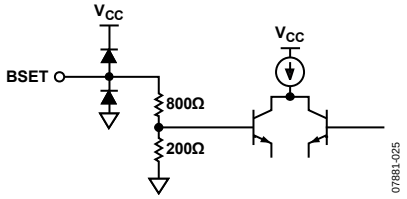

Figure 26. Equivalent Circuit of the BSET Pin

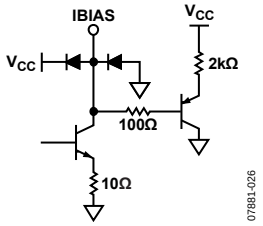

Figure 27. Equivalent Circuit of the IBIAS Pin

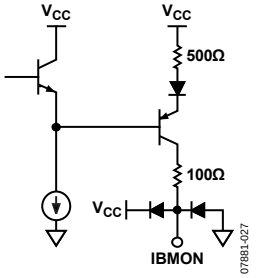

Figure 28. Equivalent Circuit of the IBMON Pin

The recommended configuration for the BSET, IBIAS, and IBMON pins is shown in Figure 29.

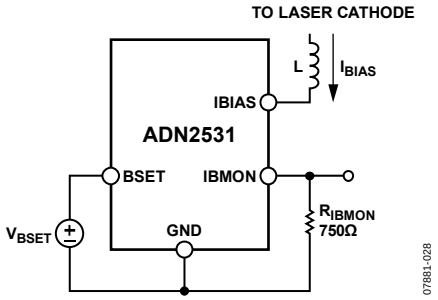

Figure 29. Recommended Configuration for BSET, IBIAS, and IBMON Pins

The circuit that drives the BSET voltage must be able to drive the 1 kΩ input resistance of the BSET pin. For proper operation of the bias current source, the voltage at the IBIAS pin must be between the compliance voltage specifications for this pin over supply, temperature, and bias current range (see Table 1). The maximum compliance voltage is specified for only two bias current levels (10 mA and 100 mA), but it can be calculated for any bias current by

$$V_{COMPLIANCE}\ (\text{V}) = V_{CC}\ (\text{V}) - 0.75 - 4.4 \times I_{BIAS}\ (\text{A})$$

See the Headroom Calculations section for examples.

The function of Inductor L is to isolate the capacitance of the IBIAS output from the high frequency signal path. For recommended components, see Table 6.

AUTOMATIC LASER SHUTDOWN (ALS)

The ALS pin is a digital input that enables/disables both the bias and modulation currents, depending on the logic state applied, as shown in Table 5.

Table 5. ALS Logic States

ALS Logic State	I_{BIAS} and I_{MOD}
High	Disabled
Low	Enabled
Floating	Enabled

The ALS pin is compatible with 3.3 V CMOS and LVTTL logic levels. The equivalent circuit is shown in Figure 30.

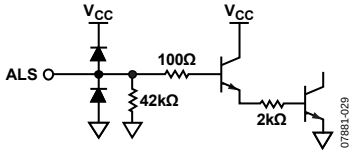

Figure 30. Equivalent Circuit of the ALS Pin

MODULATION CURRENT

The modulation current can be controlled by applying a dc voltage to the MSET pin. This voltage is converted into a dc current via a voltage-to-current converter that uses an operational amplifier and a bipolar transistor, as shown in Figure 31.

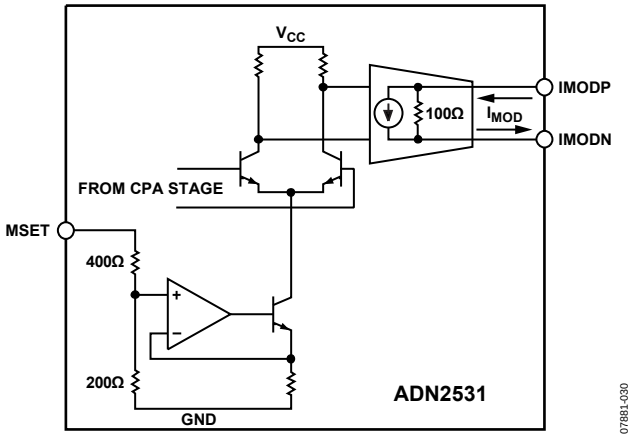

Figure 31. Generation of Modulation Current on the ADN2531

The dc current is switched by the data signal applied to the input stage (DATAP and DATAN pins) and gained up by the output stage to generate the differential modulation current at the IMODP and IMODN pins. The output stage also generates the active back-termination, which provides proper transmission line termination. Active back-termination uses feedback around an active circuit to synthesize a broadband termination resistance. This provides excellent transmission line termination while dissipating less power than a traditional resistor passive back-termination. No portion of the modulation current flows in the active back-termination resistance. All of the preset modulation current (I_{MOD}), the range of which is specified in Table 1, flows into the external load.

The equivalent circuits for the MSET, IMODP, and IMODN pins are shown in Figure 32 and Figure 33. The two 50 Ω resistors in Figure 33 represent the active back-termination resistance.

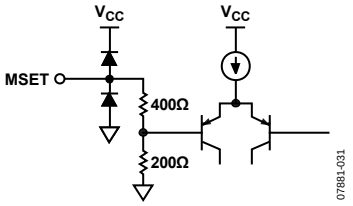

Figure 32. Equivalent Circuit of the MSET Pin

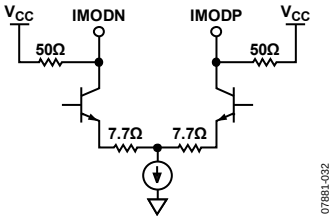

Figure 33. Equivalent Circuit of the IMODP and IMODN Pins

The recommended configuration of the MSET, IMODP, and IMODN pins is shown in Figure 34. See Table 6 for recommended components. When the voltage on DATAP is greater than the voltage on DATAN, the modulation current flows into the IMODP pin and out of the IMODN pin, generating an optical Logic 1 level at the TOSA output when the TOSA is connected as shown in Figure 34.

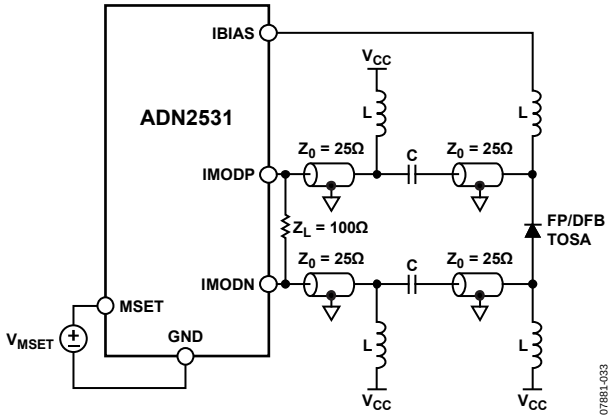

Figure 34. Recommended Configuration for the MSET, IMODP, and IMODN Pins

The ratio between the voltage applied to the MSET pin and the differential modulation current available at the IMODP and IMODN pins is a function of the load resistance value, as shown in Figure 35.

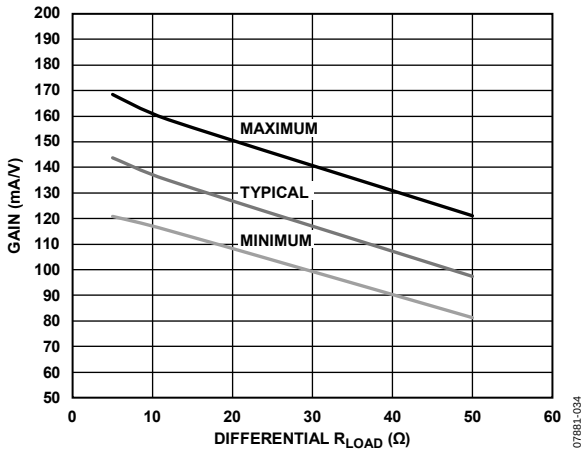

Figure 35. MSET Voltage to Modulation Current Ratio vs. Differential Load Resistance

Using the resistance of the TOSA, the user can calculate the voltage range that must be applied to the MSET pin to generate the required modulation current range (see the example in the Applications Information section).

The circuit that drives the MSET voltage must be able to drive the 600 Ω resistance of the MSET pin. To be able to drive 80 mA modulation currents through the differential load, the output stage of the ADN2531 (IMODP and IMODN pins) must be ac-coupled to the load. The voltages at these pins have a dc component equal to V_{CC} and an ac component with single-ended peak-to-peak amplitude of $I_{MOD} \times 50\ \Omega$. This is the case when the load impedance (R_{TOSA}) is less than 100 Ω differential because the transmission line characteristic impedance sets the peak-to-peak amplitude. For the case where R_{TOSA} is greater than 100 Ω, the single-ended, peak-to-peak amplitude is $I_{MOD} \times R_{TOSA} \div 2$.

For proper operation of the output stage, the voltages at the IMODP and IMODN pins must be between the compliance voltage specifications for this pin over supply, temperature, and modulation current range, as shown in Figure 36. See the Headroom Calculations section for examples of headroom calculations.

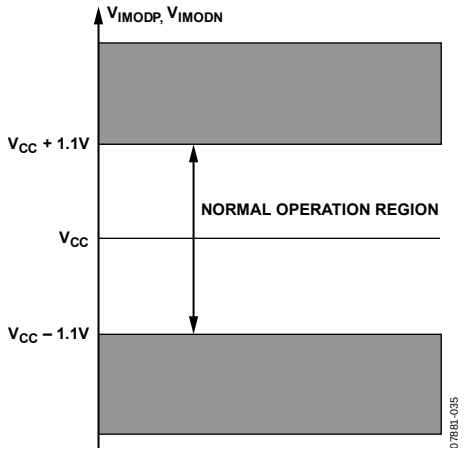

Figure 36. Allowable Range for the Voltage at IMODP and IMODN

LOAD MISTERMINATION

Due to excellent S22 performance, the ADN2531 can drive differential loads that range from 5 Ω to 140 Ω. In practice, many TOSAs have differential resistance not equal to 100 Ω. In this case, with 100 Ω differential transmission lines connecting the ADN2531 to the load, the load end of the transmission lines are misterminated. This mistermination leads to signal reflections back to the driver. The excellent back-termination in the ADN2531 absorbs these reflections, preventing reflection back to the load. This enables excellent optical eye quality to be achieved even when the load end of the transmission lines is significantly mis-terminated. The connection between the load and the ADN2531 must be made with 100 Ω differential (50 Ω single-ended) transmission lines so that the driver end of the transmission lines is properly terminated.

CROSSPOINT ADJUST

The crossing level in the output electrical eye diagram can be adjusted between 35% and 65% using the crosspoint adjust (CPA) control input. This can compensate for asymmetry in the laser response and to optimize the optical eye mask margin. The CPA input is a voltage-control input, and a plot of eye crosspoint vs. CPA control voltage is shown in Figure 14 and Figure 15 in the Typical Performance Characteristics section. The equivalent circuit for the CPA pin is shown in Figure 37. To disable the crosspoint adjust function and set the eye crossing to 50%, the CPA pin must be tied to V_{CC}.

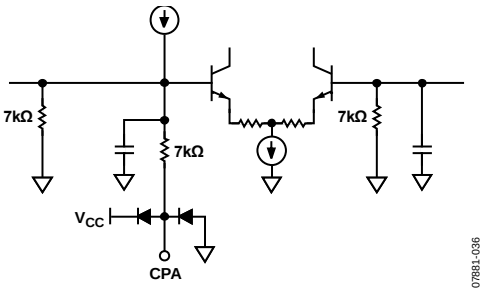

Figure 37. Equivalent Circuit for CPA Pin

POWER CONSUMPTION

The power dissipated by the ADN2531 is given by

$$P = V_{CC} \times \left(\frac{V_{MSET}}{5.8} + I_{SUPPLY} \right) + V_{IBIAS} \times I_{BIAS}$$

where:
V_{CC} is the power supply voltage.
I_{BIAS} is the bias current generated by the ADN2531.
V_{MSET} is the voltage applied to the MSET pin.
I_{SUPPLY} is the sum of the current that flows into the VCC, IMODP, and IMODN pins when $V_{BSET} = V_{MSET} = 0$ (see Table 1).
V_{IBIAS} is the average voltage on the IBIAS pin.

Considering V_{BSET}/I_{BIAS} = 10 V/A as the conversion factor from V_{BSET} to IBIAS, the dissipated power becomes

$$P = V_{CC} \times \left(\frac{V_{MSET}}{5.8} + I_{SUPPLY} \right) + V_{IBIAS} \times \left(\frac{V_{BSET}}{10V/A} \right)$$

To ensure long-term reliable operation, the ADN2531 junction temperature must not exceed 150°C, as specified in Table 3. For improved heat dissipation, the module case can be used as a heat sink, as shown in Figure 38.

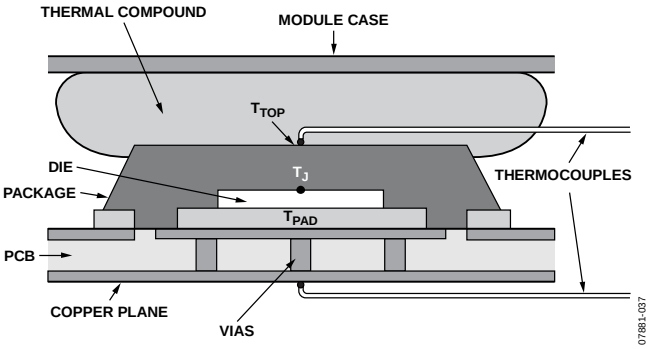

Figure 38. Typical Optical Module Structure

A compact optical module is a complex thermal environment, and calculations of device junction temperature using the junction to ambient thermal resistance (θ_{JA}) of the package do not yield accurate results. The following equation, derived from the model in Figure 39, can estimate the IC junction temperature:

$$T_J = \frac{P \times (\theta_{J-PAD} \times \theta_{J-TOP}) + T_{TOP} \times \theta_{J-PAD} + T_{PAD} \times \theta_{J-TOP}}{\theta_{J-PAD} + \theta_{J-TOP}}$$

where:
T_{TOP} is the temperature at the top of the package in °C.
T_{PAD} is the temperature at the package exposed paddle in °C.
T_J is the IC junction temperature in °C.
P is the ADN2531 power dissipation in watts.
$\theta_{J\text{-}TOP}$ is the thermal resistance from the IC junction to the top of the package.
$\theta_{J\text{-}PAD}$ is the thermal resistance from the IC junction to the exposed paddle of the package.

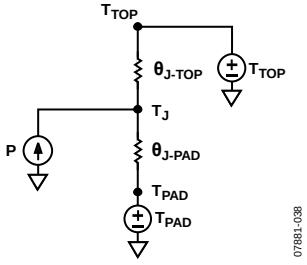

Figure 39. Electrical Model for Thermal Calculations

T_{TOP} and T_{PAD} can be determined by measuring the temperature at points inside the module, as shown in Figure 38. The thermocouples must be positioned to obtain an accurate measurement of the temperatures of the package top and paddle. $\theta_{J\text{-}TOP}$ and $\theta_{J\text{-}PAD}$ are given in Table 2.

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

Figure 40 shows a typical application circuit for the ADN2531. The dc voltages applied to the BSET and MSET pins control the bias and modulation currents. The bias current can be monitored as a voltage drop across the 750 Ω resistor connected between the IBMON pin and GND. The dc voltage applied to the CPA pin controls the crosspoint in the output eye diagram. By tying the CPA pin to V_{CC}, the CPA function is disabled. The ALS pin allows the user to turn the bias and modulation currents on and off, depending on the logic level applied to the pin. The data signal source must be connected to the DATAP and DATAN pins of the ADN2531 using 50 Ω transmission lines. The modulation current outputs, IMODP and IMODN, must be connected to the load (TOSA) using 100 Ω differential (50 Ω single-ended) transmission lines.

Table 6 provides a list of recommended components for the ac coupling interface between the ADN2531 and the TOSA. The reference circuit can support up to 11.3 Gbps applications, and the low frequency cutoff performance is dependent on the dc blocking capacitance and the transmission line impedance.

For additional applications information and optical eye diagram performance data, consult the relevant application notes on the ADN2531 product page at www.analog.com.

Table 6. Recommended Components

Component	Value	Description
R1, R2	110 Ω	0603 size resistor
R3, R4	300 Ω	0603 size resistor
R13, R14	Varies	The resistor value and size are TOSA load impedance dependent
C3, C4	100 nF	0402 size capacitor, Phycomp 223878719849
L6, L7	160 nH	0603 size inductor, Murata LQW18ANR16
L2, L3		0603 size chip ferrite bead, Murata BLM18HG601
L1, L4, L5, L8	10 µH	0805 size inductor, Murata LQM21FN100M70L

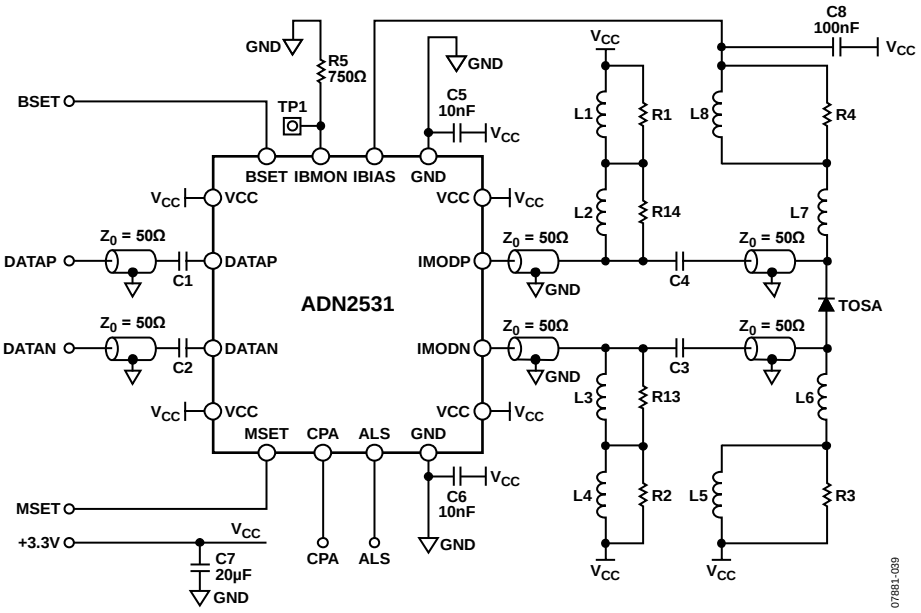

Figure 40. Typical ADN2531 Application Circuit

LAYOUT GUIDELINES

Due to the high frequencies at which the ADN2531 operates, care must be taken when designing the PCB layout to obtain optimum performance. For example, use controlled impedance transmission lines for high speed signal paths, and keep the length of transmission lines as short as possible to reduce losses and pattern-dependent jitter. In addition, the PCB layout must be symmetrical, both on the DATAP and DATAN inputs and on the IMODP and IMODN outputs, to ensure a balance between the differential signals.

Furthermore, all VCC and GND pins must be connected to solid copper planes by using low inductance connections. When these connections are made through vias, multiple vias can be connected in parallel to reduce the parasitic inductance. Each GND pin must be locally decoupled to VCC with high quality capacitors (see Figure 40). If proper decoupling cannot be achieved using a single capacitor, use multiple capacitors in parallel for each GND pin. A 20 µF tantalum capacitor must be used as the general decoupling capacitor for the entire module.

For recommended PCB layouts, including those suitable for the SFP+ and XFP modules, contact sales. For guidelines on the surface-mount assembly of the ADN2531, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, on www.analog.com.

DESIGN EXAMPLE

Assuming that the impedance of the TOSA is 12 Ω, the forward voltage of the laser at low current is V_F = 1.5 V, I_{BIAS} = 40 mA, I_{MOD} = 40 mA, and V_{CC} = 3.3 V, this design example calculates

- The headroom for the IBIAS, IMODP, and IMODN pins.
- The typical voltage required at the BSET and MSET pins to produce the desired bias and modulation currents.
- The I_{BIAS} monitor accuracy over the I_{BIAS} current range.

Headroom Calculations

To ensure proper device operation, the voltages on the IBIAS, IMODP, and IMODN pins must meet the compliance voltage specifications in Table 1.

Considering the typical application circuit shown in Figure 40, the voltage at the IBIAS pin can be written as

$$V_{IBIAS} = V_{CC} - V_F - (I_{BIAS} \times R_{TOSA}) - V_{LA}$$

where:
V_{CC} is the supply voltage.
V_F is the forward voltage across the laser at low current.
R_{TOSA} is the resistance of the TOSA.
V_{LA} is the dc voltage drop across L5, L6, L7, and L8.

For proper operation, the minimum voltage at the IBIAS pin must be greater than 0.6 V, as specified by the minimum IBIAS compliance specification in Table 1.

Assuming that the voltage drop across the 50 Ω transmission lines is negligible and that V_{LA} = 0 V, V_F = 1.5 V, and I_{BIAS} = 40 mA,

$$V_{IBIAS} = 3.3 - 1.5 - (0.04 \times 12) = 1.32 \text{ V}$$

Therefore, V_{IBIAS} = 1.32 V > 0.6 V, which satisfies the requirement

The maximum voltage at the IBIAS pin must be less than the maximum IBIAS compliance specification as described by

$$V_{COMPLIANCE\_MAX} = V_{CC} - 0.75 - 4.4 \times I_{BIAS} \text{ (A)}$$

For this example,

$$V_{COMPLIANCE\_MAX} = V_{CC} - 0.75 - 4.4 \times 0.04 = 2.374 \text{ V}$$

Therefore, V_{IBIAS} = 1.32 V < 2.374 V, which satisfies the requirement.

To calculate the headroom at the modulation current pins (IMODP and IMODN), the voltage has a dc component equal to V_{CC} due to the ac-coupled configuration and a swing equal to I_{MOD} × 50 Ω because R_{TOSA} is less than 100 Ω. For proper operation of the ADN2531, the voltage at each modulation output pin must be within the normal operation region shown in Figure 36.

Assuming the dc voltage drop across L1, L2, L3, and L4 is 0 V and I_{MOD} is 40 mA, the minimum voltage at the modulation output pins is equal to

$$V_{CC} - (I_{MOD} \times 12)/2 = V_{CC} - 0.24 \text{ V}$$

Therefore, V_{CC} − 0.24 > V_{CC} − 1.1 V, which satisfies the requirement.

The maximum voltage at the modulation output pins is equal to

$$V_{CC} + (I_{MOD} \times 12)/2 = V_{CC} + 0.24 \text{ V}$$

Therefore, V_{CC} + 0.24 < V_{CC} + 1.1 V, which satisfies the requirement.

Headroom calculations must be repeated for the minimum and maximum values of the required I_{BIAS} and I_{MOD} ranges to ensure proper device operation over all operating conditions.

BSET and MSET Pin Voltage Calculations

To set the desired bias and modulation currents, the BSET and MSET pins of the ADN2531 must be driven with the appropriate dc voltage. The voltage range required at the BSET pin to generate the required I_{BIAS} range can be calculated using the BSET voltage to I_{BIAS} gain specified in Table 1. Assuming that I_{BIAS} = 40 mA and that I_{BIAS}/V_{BSET} = 100 mA/V (which is the typical I_{BIAS}/V_{BSET} ratio), the BSET voltage is given by

$$V_{BSET} = \frac{I_{BIAS} \text{ (mA)}}{100 \text{ mA/V}} = \frac{40}{100} = 0.4 \text{ V}$$

The BSET voltage range can be calculated using the required I_{BIAS} range and the minimum and maximum BSET voltage to I_{BIAS} gain values specified in Table 1.

The voltage required at the MSET pin to produce the desired modulation current can be calculated using

$$V_{MSET} = \frac{I_{MOD}}{K}$$

where K is the MSET voltage to I_{MOD} ratio.

The value of K depends on the actual resistance of the TOSA and can be obtained from Figure 35. For a TOSA resistance of 12 Ω, the typical value of K is 110 mA/V. Assuming that I_{MOD} = 40 mA and using the preceding equation, the MSET voltage is given by

$$V_{MSET} = \frac{I_{MOD}\ (\text{mA})}{110\ \text{mA/V}} = \frac{40}{110} = 0.36\ \text{V}$$

The MSET voltage range can be calculated using the required I_{MOD} range and the minimum and maximum K values. These values can be obtained from the minimum and maximum curves in Figure 35.

IBIAS Monitor Accuracy Calculations

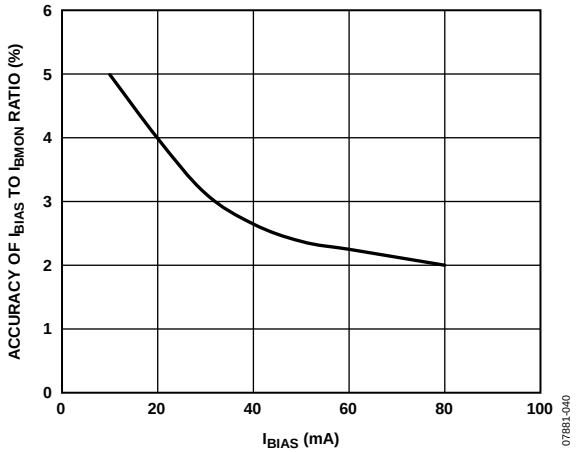

Figure 41. Accuracy of I_{BIAS} to I_{BMON} Ratio

This example assumes that the nominal value of I_{BIAS} is 40 mA and that the I_{BIAS} range for all operating conditions is 10 mA to 80 mA. The accuracy of the I_{BIAS} to I_{BMON} ratio is given in Table 1 and is plotted in Figure 41.

Referring to Figure 41, the IBMON output current accuracy is ±4.3% for the minimum I_{BIAS} of 10 mA and ±3.0% for the maximum I_{BIAS} value of 80 mA.

The accuracy of the IBMON output current as a percentage of the nominal I_{BIAS} is given by

$$IBMON\_Accuracy_{MIN} = 10\ \text{mA}\frac{4.3}{100}\times\frac{100}{40\ \text{mA}} = \pm 1.075\%$$

for the minimum I_{BIAS} value, and by

$$IBMON\_Accuracy_{MAX} = 80\ \text{mA}\frac{3.0}{100}\times\frac{100}{40\ \text{mA}} = \pm 6.0\%$$

for the maximum I_{BIAS} value. This gives a worse-case accuracy for the IBMON output current of ±6.0% of the nominal I_{BIAS} value over all operating conditions. The IBMON output current accuracy numbers can be combined with the accuracy numbers for the 750 Ω IBMON resistor (R_{IBMON}) and any other error sources to calculate an overall accuracy for the IBMON voltage.

OUTLINE DIMENSIONS

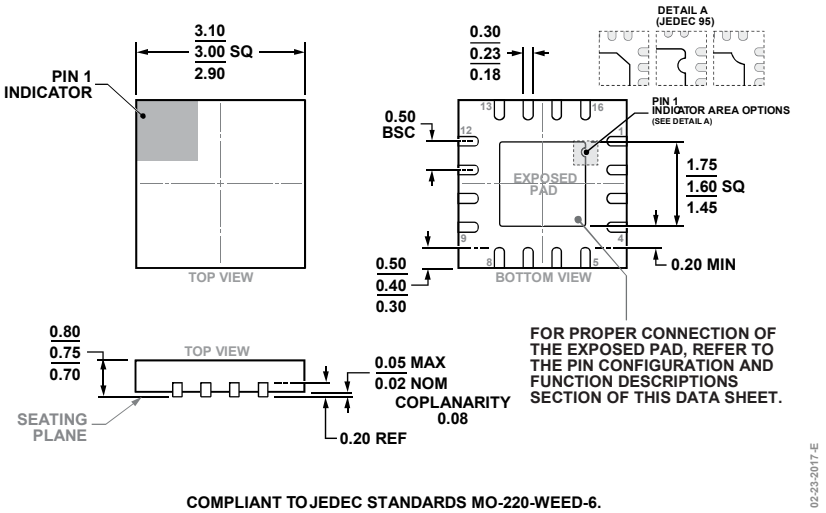

Figure 42. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADN2531ACPZ	−40°C to +100°C	16-Lead LFCSP	CP-16-22	F0K
ADN2531ACPZ-R7	−40°C to +100°C	16-Lead LFCSP, 1,500-Piece Reel	CP-16-22	F0K
EVAL-ADN2531-NTZ		Optical Evaluation Board Without Laser Populated		

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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